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1. (Currently Amended) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material; and

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially.

2. (Original) The method of claim 1 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal; and

selecting a second temperature, a second pressure, and a second time for the oxygen-based anneal.

3. (Original) The method of claim 2 wherein the first temperature is selected from a range between about 500 °C and about 1000 °C, the first pressure is selected from a range between about 0.1 torr and about 760 torr, and the first time is selected from a range between about 10 seconds and about 10 minutes.

4. (Original) The method of claim 3 wherein the first temperature is about 800 °C, the first pressure is about 40 torr, and the first time is about 1 minute.

5. (Original) The method of claim 2 wherein the second temperature is selected from a range between about 700 °C and about 900 °C, the second pressure is selected from a range between about 1 millitorr and about 10 torr, and the second time is selected from a range between about 1 second and about 300 seconds.

6. (Original) The method of claim 1 further comprising selecting a first chemical for the hydrogen-based anneal and a second chemical for the oxygen-based anneal, wherein the first and second chemicals are selected based on a chemical composition of the high-k material.

7. (Original) The method of claim 6 wherein the first chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH4.

8. (Original) The method of claim 6 wherein the second chemical is selected from the group consisting of:

O_2;

N_2O;

NO; and

D_2O.

9. (Original) The method of claim 1 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

10. (Original) The method of claim 9 wherein the high-k material is HfO_2, and wherein the method further comprises selecting an HfO_2 deposition temperature from a range between about 200 °C and about 400 °C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

11. (Original) The method of claim 10 wherein a plurality of cycles of the ALD process are performed until the selected deposition depth is attained.

12. (Original) The method of claim 1 wherein the substrate comprises diamond.

13. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

placing a pseudo-substrate in a process reactor;
applying a loading treatment to the pseudo-substrate;
removing the pseudo-substrate from the process reactor;
placing a device substrate into the process reactor; and
forming a poly-silicon layer upon the device substrate.

14. (Original) The method of claim 13 wherein the pseudo-substrate comprises a material selected from the group consisting of:

silicon; and
diamond.

15. (Original) The method of claim 13 further comprising:

selecting a first temperature, a first pressure, and a first time for the loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

16. (Original) The method of claim 15 wherein the first temperature is selected from a range between about 550 °C and about 750 °C, the first pressure is selected from a range between about 0.1 torr and about 80 torr, and the first time is selected from a range between about 1 second and about 5 minutes.

17. (Original) The method of claim 16 wherein the first temperature is about 625 °C, the first pressure is about 40 torr, and the first time is about 1 minute.

18. (Original) The method of claim 15 wherein the second temperature is selected from a range between about 700 °C and about 900 °C, the second pressure is selected from a range between about 1 millitorr and about 760 torr, and the second time is selected from a range between about 1 second and about 20 minutes.

19. (Original) The method of claim 13 further comprising selecting a chemical for the loading treatment.

20. (Original) The method of claim 19 wherein the chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

21. (Original) The method of claim 13 wherein the loading treatment is performed within the same process environment as the poly-silicon formation.

22. (Original) The method of claim 13 wherein the loading treatment is performed within an individual process environment.

23. (Original) The method of claim 13 wherein the loading treatment employs a plasma.

24. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material;

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially;

applying a loading treatment to the high-k material; and

forming a poly-silicon layer on the treated high-k material, wherein the loading treatment and poly-silicon deposition occur sequentially.

25. (Currently Amended) The method of claim 24 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal;

selecting a second temperature, a second pressure, and a second time for the oxygen-based ~~anneal.~~ anneal;

selecting a third temperature, a third pressure, and a third time for the loading treatment; and

selecting a fourth temperature, a fourth pressure, and a fourth time for the poly-silicon layer formation.

26. (Original) The method of claim 25 wherein the first temperature is selected from a range between about 500 °C and about 1000 °C, the first pressure is selected from a range between about 0.1 torr and about 760 torr, and the first time is selected from a range between about 10 seconds and about 10 minutes.

27. (Original) The method of claim 26 wherein the first temperature is about 800 °C, the first pressure is about 40 torr, and the first time is about 1 minute.

28. (Original) The method of claim 25 wherein the second temperature is selected from a range between about 700 °C and about 900 °C, the second pressure is selected from a range between about 1 millitorr and about 10 torr, and the second time is selected from a range between about 1 second and about 300 seconds.

29. (Original) The method of claim 25 wherein the third temperature is selected from a range between about 450 °C and about 650 °C, the third pressure is selected from a range between about 0.1 torr and about 80 torr, and the third time is selected from a range between about 1 seconds and about 5 minutes.

30. (Original) The method of claim 29 wherein the third temperature is about 500 °C, the third pressure is about 40 torr, and the third time is about 2 minutes.

31. (Original) The method of claim 25 wherein the fourth temperature is selected from a range between about 700 °C and about 900 °C, the fourth pressure is selected from a range between about 1 millitorr and about 760 torr, and the fourth time is selected from a range between about 1 second and about 20 minutes.

32. (Original) The method of claim 24 further comprising selecting a first chemical for the hydrogen-based anneal, a second chemical for the oxygen-based anneal, and a third chemical for the loading treatment, wherein the first, second, and third chemicals are selected based on a chemical composition of the high-k material.

33. (Original) The method of claim 32 wherein the first chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

34. (Original) The method of claim 32 wherein the second chemical is selected from the group consisting of:

O_2;

N_2O;

NO; and

D_2O.

35. (Original) The method of claim 24 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

36. (Original) The method of claim 35 wherein the high-k material is HfO_2, and wherein the method further comprises selecting a HfO_2 deposition temperature from a range between about 200 °C and about 400 °C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

37. (Original) The method of claim 35 wherein a plurality of cycles of the ALD process are performed until a selected deposition depth is attained.

38. (Original) The method of claim 24 wherein the loading treatment is performed within the same process environment of the poly-silicon formation.

39. (Original) The method of claim 24 wherein the loading treatment is performed within an individual process environment.

40. (Original) The method of claim 24 wherein the loading treatment employs a plasma.

41. (Original) The method of claim 24 wherein the substrate comprises diamond.

42. (Currently Amended) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate on the substrate;

depositing a high dielectric constant (high-k) material upon the thin insulate;

performing an anneal on the high-k material;

applying a hydrogen-containing gas loading treatment upon the annealed high-k material; and

forming a poly-silicon layer on the treated high-k material, wherein the ~~anneal~~ hydrogen-containing gas loading treatment and poly-silicon deposition occur sequentially.

43. (Currently Amended) The method of claim 42 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-containing gas loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

44. (Original) The method of claim 43 wherein the first temperature is selected from a range between about 450 °C and about 650 °C, the first pressure is selected from a range between about 0.1 torr and about 80 torr, and the first time is selected from a range between about 1 second and about 5 minutes.

45. (Original) The method of claim 44 wherein the first temperature is about 500 °C, the first pressure is about 40 torr, and the first time is about 2 minutes.

46. (Original) The method of claim 43 wherein the second temperature is selected from a range between about 700 °C and about 900 °C, the second pressure is selected from a range between about 1 millitorr and about 760 torr, and the second time is selected from a range between about 1 second and about 20 minutes.

47. (Currently Amended) The method of claim 42 further comprising selecting a ~~chemical~~ hydrogen-containing gas for the hydrogen-containing gas loading treatment.

48. (Currently Amended) The method of claim 47 wherein the ~~chemical~~ hydrogen-containing gas is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

49. (Currently Amended) The method of claim 42 wherein the hydrogen-containing gas loading treatment is performed within the same process environment of the poly-silicon formation. .

50. (Currently Amended) The method of claim 42 wherein the hydrogen-containing gas loading treatment is performed within an individual process environment.

51. (Currently Amended) The method of claim 42 wherein the hydrogen-containing gas loading treatment employs a plasma.

52. (Original) The method of claim 42 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

53. (Original) The method of claim 52 wherein the high-k material is HfO_2, and wherein the method further comprises selecting an HfO_2 deposition temperature from a range between about 200 °C and about 400 °C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

54. (Original) The method of claim 52 wherein a plurality of cycles of the ALD process are performed until a selected deposition depth is attained.

55. (Original) The method of claim 42 wherein the substrate comprises diamond.

15. (Original) A non-volatile memory according to Claim 14, wherein a rough surface is provided on the metal-oxide layer in the region where it comes into contact with the phase-change recording medium.

16. (Original) A non-volatile memory according to Claim 15, wherein the surface region where the metal-oxide layer comes into contact with the phase-change recording medium has an average roughness (Ra) not smaller than 10 nm to not greater than 100 nm.

17. (Original) A non-volatile memory according to Claim 15, wherein

the metal-oxide layer has a multi-layered structure comprising a first oxide conductive film that has a small average grain size or that is amorphous and a second oxide conductive film that has an average grain size greater than that of the first oxide conductive film; and

the surface of the second oxide conductive film is structured so as to contact with the phase-change recording medium.

18. (Original) A non-volatile memory according to Claim 13, which further comprises an insulating tube that is formed along the inner surface of the throughhole and that has a thermal conductivity lower than that of the insulating layer.

19. (Withdrawn) A method for fabricating a non-volatile memory comprising the steps of:

forming a first electrode that contains as a main ingredient at least one member selected from the group consisting of ruthenium, rhodium and osmium on a substrate having an insulator in between;

-15. (Original) A non-volatile memory according to Claim 14, wherein a rough surface is provided on the metal-oxide layer in the region where it comes into contact with the phase-change recording medium.

16. (Original) A non-volatile memory according to Claim 15, wherein the surface region where the metal-oxide layer comes into contact with the phase-change recording medium has an average roughness (Ra) not smaller than 10 nm to not greater than 100 nm.

17. (Original) A non-volatile memory according to Claim 15, wherein

the metal-oxide layer has a multi-layered structure comprising a first oxide conductive film that has a small average grain size or that is amorphous and a second oxide conductive film that has an average grain size greater than that of the first oxide conductive film; and

the surface of the second oxide conductive film is structured so as to contact with the phase-change recording medium.

18. (Original) A non-volatile memory according to Claim 13, which further comprises an insulating tube that is formed along the inner surface of the throughhole and that has a thermal conductivity lower than that of the insulating layer.

forming an insulating layer on the first electrode;

forming a throughhole in the insulating layer by photolithography;

forming a phase-change recording medium that comprises a standing portion filling in the throughhole and a layered portion formed on the surface of the insulating layer by depositing a phase-change material containing chalcogen(s) on the insulating layer; and

forming a second electrode that contains as a main ingredient at least one member selected from the group consisting of ruthenium, rhodium and osmium on the phase-change recording medium.

20. (Withdrawn) A method for fabricating a non-volatile memory according to Claim 19, which further comprises a step for forming a first metal-oxide layer between the steps for forming the throughhole and forming the phase-change recording medium, wherein

the formation of the first metal-oxide layer is conducted by oxidizing the portion of the first electrode exposed by the throughhole.

21. (Withdrawn) A method for fabricating a non-volatile memory according to Claim 19, which further comprises a step for forming a second metal-oxide layer between the steps for forming the phase-change recording medium and forming the second electrode, wherein

the second metal-oxide layer and the second electrode are formed by sequential sputtering under an oxygen atmosphere and under an inert gas atmosphere respectively in the same sputtering apparatus.

1. (Currently Amended) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

cleaning the surface of the substrate;

forming a thin insulate over the substrate;

depositing a high dielectric constant (high-k) material over the thin insulate;

performing a hydrogen-based anneal on the high-k material; and

performing an oxygen-based anneal on the high-k material, wherein the hydrogen-based and oxygen-based anneals occur sequentially.

2. (Original) The method of claim 1 further comprising:

selecting a first temperature, a first pressure, and a first time for the hydrogen-based anneal; and

selecting a second temperature, a second pressure, and a second time for the oxygen-based anneal.

3. (Original) The method of claim 2 wherein the first temperature is selected from a range between about 500 °C and about 1000 °C, the first pressure is selected from a range between about 0.1 torr and about 760 torr, and the first time is selected from a range between about 10 seconds and about 10 minutes.

4. (Original) The method of claim 3 wherein the first temperature is about 800 °C, the first pressure is about 40 torr, and the first time is about 1 minute.

5. (Original) The method of claim 2 wherein the second temperature is selected from a range between about 700 °C and about 900 °C, the second pressure is selected from a range between about 1 millitorr and about 10 torr, and the second time is selected from a range between about 1 second and about 300 seconds.

6. (Original) The method of claim 1 further comprising selecting a first chemical for the hydrogen-based anneal and a second chemical for the oxygen-based anneal, wherein the first and second chemicals are selected based on a chemical composition of the high-k material.

7. (Original) The method of claim 6 wherein the first chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH4.

8. (Original) The method of claim 6 wherein the second chemical is selected from the group consisting of:

O_2;

N_2O;

NO; and

D_2O.

9. (Original) The method of claim 1 wherein the high-k material is deposited using an atomic layer deposition (ALD) process.

10. (Original) The method of claim 9 wherein the high-k material is HfO_2, and wherein the method further comprises selecting an HfO_2 deposition temperature from a range between about 200 °C and about 400 °C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

11. (Original) The method of claim 10 wherein a plurality of cycles of the ALD process are performed until the selected deposition depth is attained.

12. (Original) The method of claim 1 wherein the substrate comprises diamond.

13. (Original) A method for fabricating a portion of an integrated circuit on a semiconductor substrate, the method comprising:

placing a pseudo-substrate in a process reactor;
applying a loading treatment to the pseudo-substrate;
removing the pseudo-substrate from the process reactor;
placing a device substrate into the process reactor; and
forming a poly-silicon layer upon the device substrate.

14. (Original) The method of claim 13 wherein the pseudo-substrate comprises a material selected from the group consisting of:

silicon; and
diamond.

15. (Original) The method of claim 13 further comprising:

selecting a first temperature, a first pressure, and a first time for the loading treatment; and

selecting a second temperature, a second pressure, and a second time for the poly-silicon layer formation.

16. (Original) The method of claim 15 wherein the first temperature is selected from a range between about 550 °C and about 750 °C, the first pressure is selected from a range between about 0.1 torr and about 80 torr, and the first time is selected from a range between about 1 second and about 5 minutes.

17. (Original) The method of claim 16 wherein the first temperature is about 625 °C, the first pressure is about 40 torr, and the first time is about 1 minute.

18. (Original) The method of claim 15 wherein the second temperature is selected from a range between about 700 °C and about 900 °C, the second pressure is selected from a range between about 1 millitorr and about 760 torr, and the second time is selected from a range between about 1 second and about 20 minutes.

19. (Original) The method of claim 13 further comprising selecting a chemical for the loading treatment.

20. (Original) The method of claim 19 wherein the chemical is selected from the group consisting of:

H_2;

NH_3; and

SiH_4.

21. (Original) The method of claim 13 wherein the loading treatment is performed within the same process environment as the poly-silicon formation.

22. (Original) The method of claim 13 wherein the loading treatment is performed within an individual process environment.

23. (Original) The method of claim 13 wherein the loading treatment employs a plasma.

53. (Original) The method of claim 52 wherein the high-k material is HfO_2, and wherein the method further comprises selecting an HfO_2 deposition temperature from a range between about 200 °C and about 400 °C, and selecting a deposition depth from a range between about 3 Angstroms and about 75 Angstroms.

54. (Original) The method of claim 52 wherein a plurality of cycles of the ALD process are performed until a selected deposition depth is attained.

55. (Original) The method of claim 42 wherein the substrate comprises diamond.